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Attorney's Docket No. 67,200-327 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Liang et al
Serial No.: 09/ 885,784
Filed: June 20, 2001
For: Laminating Method for Fabricating Integrated Circuit Microelectronic Fabrication

Group Art Unit: 2823
Examiner: Julio J. Maldanado

Commissioner for Patents
Alexandria, VA 22313

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on Oct. 8, 2003.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

___	small entity	$165.00
X	other than a small entity	$330.00

Appeal Brief fee due: $ 330.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing
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for Patents, Alexandria, VA 22313

Dated: 10-30-03

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 420.00	$210.00
☐	three months	$ 950.00	$475.00
☐	four months	$1,480.00	$740.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 330.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 330.00

6. FEE PAYMENT

X Attached is a Credit Card Payment Form for the sum of $ 330.00
X Credit Card Payment Form in the sum of $ 330.00 .
A duplicate copy of this transmittal is attached.

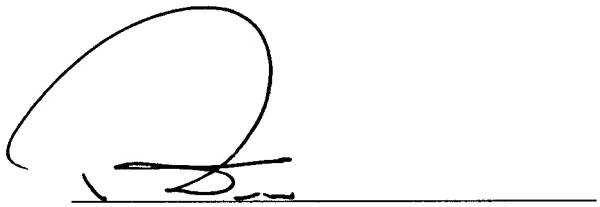
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

__X__ If any additional extension and/or fee is required, this is a request therefor to charge Deposit Account No. __50-0484__

And/Or

__X__ If any additional fee for claims is required, please charge Deposit Account No. __50-0484__



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67,200-327; TSMC 00-132
Serial Number 09/885,784

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FROM: Tung & Associates
838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302

DATE: 27 October 2003

REF:

Appellant	:	Liang et al.	Filing Date	:	20 June 2001
Serial No..	:	09/885,784	Att'y No.	:	67,200-327; TSMC 00-132
Art Unit	:	2823	Examiner	:	Julio J. Maldanado
Title	:	Laminating Method for Fabricating Integrated Circuit Microelectronic Fabrication			

EXPRESS MAIL CERTIFICATE

Express Mail label Number EL 995 797 525 US
Date of Deposit Oct. 30, 2003

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $320.00 (required filing fee) are being deposited with the United States Postal Service via Express Mail on the date indicated above and is addressed to: Mail Stop: Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Kathy Dixon

APPEAL BRIEF

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 8 July 2003 and made FINAL, appellant filed a notice of appeal on 8 October 2003. In accord with appellant's notice of appeal, please accept this appeal brief. No oral argument is requested.

1. Real Party in Interest

The real party in interest for this application is the assignee:

Taiwan Semiconductor Manufacturing Co., Ltd.
121 Park Avenue, No. 3
Science Based Industrial Park
Hsin-Chu, Taiwan, Republic of China

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims

Claims 2-8, 12-13 and 16 are pending in this application. Claims 1, 9-11 and 14-15 have been canceled. No claims have been allowed, objected to or subject to restriction. Claims 2-8, 12-13 and 16 are finally rejected under 35 U.S.C. § 103(a).

4. Status of the Amendments

A reply, filed 7 September 2003, was submitted in response to the office action made FINAL, in order to overcome the Examiner's rejections of the claims pending within this application. In an advisory action mailed on 2 October 2003, the Examiner indicated that appellant's request for reconsideration was considered by did not place appellant's application in condition for allowance, for reasons related to those of record.

5. Summary of the Invention

The invention provides a method for efficiently fabricating a microelectronic fabrication. The invention realizes the foregoing object by employing when fabricating a semiconductor integrated circuit microelectronic fabrication: (1) a partially fabricated semiconductor integrated circuit microelectronic fabrication formed from a first semiconductor

substrate having a minimum of one semiconductor device fabricated thereover, wherein the partially fabricated semiconductor integrated circuit microelectronic fabrication is laminated with; (2) a second substrate having formed thereover a dielectric isolated metallization pattern to mate the dielectric isolated metallization pattern with the partially fabricated semiconductor integrated circuit microelectronic fabrication. By employing within the context of the present invention a first semiconductor substrate and a separate second substrate, each partially fabricated with respect to a semiconductor integrated circuit microelectronic fabrication, and laminating the first semiconductor substrate and the second substrate to provide a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication, the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication may be formed with enhanced efficiency since at least two separate portions of the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication may be fabricated in parallel. (paragraph 0015, counted by hand)

The invention is claimed in one level of scope (independent claim 16 and remaining pending claims dependent thereupon) that provides a method for fabricating a semiconductor integrated circuit microelectronic fabrication.

Independent claim 16 is read on the specification and drawings as follows (all paragraph numbers are counted by hand):

16. (previously presented) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate 10; (Fig. 1; and paragraph 0024)

forming over the first semiconductor substrate 10 at least one microelectronic device 14/16/18a/18b to form from the first semiconductor substrate 10 a partially fabricated semiconductor integrated circuit microelectronic fabrication 24; (Fig. 1; and paragraphs 0027 and 0033)

providing a second substrate 30; (Fig. 2; and paragraph 0036)

forming over the second substrate 30, in inverted order, a dielectric isolated metallization pattern 46 intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication 24; (Fig. 2; and paragraph 0038)

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication 24 with the second substrate 30 to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication 24 with the dielectric isolated metallization pattern 46 to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication 48; (Fig. 3; and paragraph 0043) and

removing the second substrate 30 from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication 48 while employing a removal method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, where the removal method employs the dielectric isolated metallization pattern 46 as a stop layer. (Fig. 4; and paragraphs 0047-0048)

6. Issues

I. Whether claims 3-7, 12-13 and 16 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly et al. (U.S. Patent No. 6,143,117; hereinafter "Kelly") in view of Mountain (U.S. Patent No. 6,013,534) and Haq (U.S. Patent No. 6,245,677).

II. Whether claim 2 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Davidson (U.S. Patent No. 5,880,010).

III. Whether claim 8 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Kresge et al. (U.S. Patent No. 6,066,808; hereinafter "Kresge").

7. Grouping of Claims

Claims 2-8, 12-13 and 16 (group I) are directed towards a single claimed embodiment of the invention.

The claims stand or fall together within group I.

8. Argument

I. Claims 3-7, 12-13 and 16 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq.

II. Claim 2 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Davidson.

III. Claim 8 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Kresge.

a. Kelly Subject Matter

Kelly (title, abstract and cover figures) teaches a laminating and releasing method for transferring a thin film structure from a first substrate carrier to a second substrate carrier. The method is related to appellant's laminating and releasing method for forming appellant's laminated completely fabricated semiconductor integrated circuit microelectronic fabrication and removing appellant's second substrate therefrom. Kelly's method effects release of a substrate

from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication by effecting interfacial disturbance, such as laser ablation or dicing.

b. Mountain Subject Matter

Mountain (title, abstract and cover figure) teaches a method for backside thinning of integrated circuit dice. The method provides for forming, in sequential process steps, a laminated structure comprising a handle wafer, an etch stop layer, an adhesive layer and a template wafer into which is received a series of dice for backside thinning. After backside thinning of the series of dice, the series of dice are backside laminated to a carrier wafer. The handle wafer, etch stop layer and adhesive layer are then removed such as to provide for frontside electrical testing of the backside thinned integrated circuit dice.

c. Haq Subject Matter

Haq (title, abstract and cover figure) teaches a backside chemical mechanical polish (CMP) planarizing method for reducing thicknesses of semiconductor substrates.

d. Davidson Subject Matter

Davidson (title, abstract and cover figure) teaches a laminating method for forming ultrathin electonics. Davidson is specifically cited at col. 3, lines 58-67 as teaching resistors, transistors, diodes and capacitors within microelectronic fabrications.

e. Kresge Subject Matter

Kresge (title, abstract and cover figure) teaches a printed circuit board having metallization pads flush with a top surface of the printed circuit board. Kresge is specifically cited at col. 7, line 45 to col. 8, line 35 as teaching lamination methods employing indium and indium alloy bonding materials when fabricating microelectronic fabrications.

f. The Examiner's Assertions

Within the paragraph bridging pages 2-3 of the office action made FINAL, the Examiner employs Kelly as a base reference that the Examiner reads against appellant's independent claim 16.

At page 3, first full paragraph of the office action made FINAL, the Examiner acknowledges that Kelly does not teach "removing [a] second substrate [from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication] while employing [a] dielectric isolated metallization pattern as an etch stop layer." (emphasis added) Rather, the Examiner at page 3, first full paragraph of the office action made FINAL relies upon Mountain at col. 5, lines 6-13 and col. 6, line 65 to col. 7, line 3 for teaching removal of a substrate from a laminated microelectronic fabrication while employing a dielectric layer as a stop layer and with a combination of chemical and mechanical processes. The Examiner rationalizes suggestion or motivation for modification or combination of Kelly's lamination method to incorporate therein Mountain's substrate removal method since Mountain's method "is a conventional process that can be used to reduce the thickness of a device and provide better handling" as taught within Mountain at col. 1, lines 36-47 and col. 6, line 65 to col. 7, line 3.

Within the paragraph bridging pages 3-4 of the office action made FINAL, the Examiner acknowledges that Kelly in view of Mountain fails to teach a method from the group selected from milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods for removing a substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication. Rather, the Examiner relies upon Haq at col. 2, line 55 to col. 4, line 8 for such a teaching. Finally, the Examiner rationalizes suggestion or motivation for modification or combination of Kelly in view of Mountain to include a substrate thinning method of Haq since the same "would reduce stress forces to the wafer during manufacturing" as disclosed within Haq at col. 2, lines 66-67.

At page 6, second paragraph of the office action made FINAL the Examiner acknowledges that Kelly in view of Mountain and Haq fails to teach a microelectronic device selected from the group consisting of resistors, transistors, diodes and capacitors within a microelectronic fabrication. Rather the Examiner relies upon Davidson at col. 3, lines 58-67 for such a teaching. The Examiner rationalizes suggestion or motivation for modification or combination of Kelly in view of Haq and Mountain to incorporate therein a microelectronic device as taught within Davidson since the same "would reduce the space of an integrated circuit to less than one percent of its conventional size" as taught within Davidson at col. 1, lines 35-39.

At page 6, fourth paragraph of the office action made FINAL the Examiner acknowledges that Kelly in view of Mountain and Haq fail to teach using thermally assisted laminating methods and pressure assisted laminating methods to mate a partially fabricated semiconductor integrated circuit microelectronic fabrication with a dielectric isolated metallization pattern using a bonding material selected from the group consisting of indium and indium alloy bonding materials. Rather, the Examiner relies upon Kresge at col. 7, line 45 to col. 8, line 35 for such a teaching. The Examiner rationalizes suggestion or motivation for modification or combination Kelly in view of Mountain and Haq to incorporate therein Kresge's pressure laminating method employing indium or indium alloy materials since the same would "promote an effective engagement between integrated circuits, and prevent dielectric intrusion through the conductive bond" as taught within Kresge at col. 8, lines 9-35.

f. Appellant's Response

In response in a first instance, appellant notes that the Examiner at page 3, first full paragraph of the office action made FINAL acknowledges that Kelly fails to teach removal of a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as an etch stop layer. However, appellant also notes that the complete limitation absent within Kelly in comparison with appellant's claim 16 is removal of the second substrate from the laminated

completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a removal method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, while employing the dielectric isolated metallization pattern as a stop layer. Thus, appellant understands both: (1) milling, polish or planarizing removal method limitations; and (2) dielectric isolated metallization pattern stop layer limitations, to be absent within Kelly and needed to properly reject applicant's claim 16 under 35 U.S.C. § 103(a) over Kelly in combination with other references.

Appellant asserts that the foregoing limitation is not taught within Mountain, as is apparently implicitly suggested by the Examiner since the Examiner at page 3, first full paragraph asserts that Mountain teaches "removing a substrate using a dielectric layer as a stop layer with combination of chemical and mechanical processes." (emphasis added) Mountain at col. 5, lines 6-7 first teaches that "a material that is suitable as an etch stop is deposited on the handle wafer." (emphasis added) Mountain at col. 5, lines 8-10 next teaches that "[t]he etch stop material may be selected from the group consisting of silicon oxide, silicon nitride, metal, polymer, silicon carbide and bisbenzocyclobutene resin (BCB)." (emphasis added)

In accord with Mountain's foregoing teachings, appellant understands Mountain to teach for use as an etch stop material in an etch stop layer a single material selected from the group consisting of metals and several dielectrics. Mountain apparently neither explicitly nor implicitly teaches an etch stop layer of a dielectric isolated metallization pattern that would of necessity comprise both a conductor (such as a metal) and a dielectric. Within Mountain's invention Mountain's etch stop layer is an extrinsic etch stop layer, apparently formed and employed only for etch stop purposes. Mountain implicitly would have no motivation to employ

a dielectric isolated metallization pattern for etch stop purposes, but rather an etch stop layer formed of a single etch stop material appears entirely adequate within Mountain's invention. Thus, appellant asserts that Mountain neither explicitly nor implicitly discloses a dielectric isolated metallization pattern as a stop layer when removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication in accord with appellant's invention as disclosed and claimed within claim 16, last clause.

With respect to the Examiner's assertion of suggestion or motivation for modification or combination of Kelly with Mountain predicated upon reduction of thickness of a microelectronic fabrication such as to provide better handling thereof, Mountain at col. 1, lines 36-47 discloses that thicker semiconductor substrates, rather than thinner semiconductor substrates, provide for better handling (i.e., less breakage) of semiconductor fabrications, inapposite to that which is asserted by the Examiner. Thus, appellant asserts that there exists no suggestion or motivation for modification or combination of Kelly with Mountain for reasons as suggested by the Examiner, since the reasons as suggested by the Examiner are not accurately reflected within portions of Mountain as cited by the Examiner.

In accord with the above, appellant thus first asserts that each and every limitation within appellant's invention as disclosed and claimed within claim 16 is neither explicitly nor implicitly disclosed within Kelly, Mountain or the combination thereof, in particular with respect to removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer. In addition, appellant second asserts that there exists no suggestion or motivation for modification or combination of Kelly with Mountain for substrate thinning and better handling reasons as cited by the Examiner, since Mountain at col. 1, lines 36-47 and col. 6, line 65 to col.

7, line 3 as cited by the Examiner teaches that thicker semiconductor substrates provide better handling.

In response in a second instance, appellant notes that Haq at col. 2, line 55 to col. 4, line 9 as cited by the Examiner, does teach a polishing method for backside thinning of a substrate such as a semiconductor substrate. Haq does not apparently require a dielectric isolated metallization pattern be formed upon Haq's substrate prior to thinning thereof, nor does Haq explicitly disclose employing the dielectric isolated metallization pattern as a stop layer when thinning Haq's substrate. Haq at col. 3, lines 18-24 teaches that Haq's invention is preferably employed with the context of "semiconductor substrates with live circuits defined on a front side thereof." Presumably, the live circuits may include a dielectric isolated metallization patterns such as to access semiconductor devices employed within the live circuits and formed within the semiconductor substrate. Under such circumstances where a semiconductor substrate having formed therein semiconductor devices and formed thereupon a dielectric isolated metallization pattern to access the semiconductor devices and live circuits formed therefrom is completely thinned and removed while employing the dielectric isolated metallization pattern as a stop layer nominally in accord with appellant's invention as disclosed and claimed within claim 16, last clause, Haq's invention is rendered inoperative for its intended purpose since such complete thinning and removal of Haq's semiconductor substrate would also remove Haq's semiconductor devices and render inoperative Haq's live circuits. Thus, in addition to not explicitly teaching each and every limitation within appellant's invention as disclosed and claimed within claim 16 with respect to removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer, Haq inherently or implicitly may not be extended to

provide that limitation since upon such extension Haq is implicitly rendered inoperative for Haq's intended purpose.

Thus, since: (1) the Examiner acknowledges that Kelly does not disclose removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer; (2) appellant asserts (as not apparently expressly contradicted by the Examiner) that Mountain does not expressly or implicitly disclose removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer; (3) there exists no suggestion or motivation for modification or combination or Kelly with Mountain for reasons as cited by the Examiner; and (4) Haq inherently or implicitly may not properly be extended to provide for removal of a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer since Haq is otherwise rendered inoperative for Haq's intended purpose, appellant asserts that at minimum each and every limitation within appellant's invention as disclosed and claimed within claim 16 is not taught within Kelly, Mountain, Haq or any combination thereof and thus at minimum claim 16 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq. Since all remaining claims within the foregoing rejections are dependent upon claim 16 and carry all of the limitations of claim 16, appellant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq.

In light of the foregoing responses, appellant respectfully requests that the Examiner's rejections of claims 3-7, 12-13 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq be reversed.

With respect to (1) the Examiner's rejection of claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Davidson; and (2) the Examiner's rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Kresge, appellant predicates patentability of claim 2 and claim 8 upon their dependence upon claim 16. Thus, appellant also respectfully requests that the Examiner's rejections of: (1) claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Davidson; and (2) claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Kresge, be reversed.

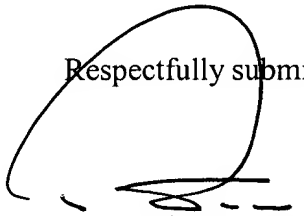
9. Summary

Appellant's invention as disclosed and claimed within claim 16 provides a laminating method for forming a microelectronic fabrication. The laminating method laminates a partially fabricated semiconductor integrated circuit microelectronic fabrication with a dielectric isolated metallization pattern formed in inverted order over a second substrate. The second substrate is then removed employing a removal method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, and while employing the dielectric isolated metallization pattern as a stop layer. Absent from the prior art of record employed in rejecting appellant's claims to appellant's invention is a teaching of each and every limitation within appellant's invention as disclosed and claimed within claim 16.

10. Conclusion

Appellant requests that the Board of Patent Appeals and Interferences reverse the Examiner's action in rejecting the claims within this application within the office action made FINAL. Allowance of all claims pending within this application, in accord with the appended copy of the claims, is respectfully requested.

Respectfully submitted,



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APPENDIX

COMPLETE COPY OF THE CLAIMS

1. (canceled)

2. (previously presented) The method of claim 16 wherein the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors.

3. (previously presented) The method of claim 16 wherein the second substrate is selected from the group consisting of conductor substrates, semiconductor substrates, dielectric substrates and aggregates thereof.

4. (previously presented) The method of claim 16 wherein the second substrate is a second semiconductor substrate.

5. (previously presented) The method of claim 16 wherein the first semiconductor substrate is thicker than the second substrate.

6. (previously presented) The method of claim 16 wherein the dielectric isolated metallization pattern comprises a plurality of laminated patterned conductor layers.

7. (original) The method of claim 6 wherein each laminated patterned conductor layer within the plurality of laminated patterned conductor layers is formed to a thickness of from about 3000 to about 6000 angstroms.

8. (previously presented) The method of claim 16 wherein the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern formed over the second substrate is undertaken while employing a laminating method selected from the group consisting of thermally assisted laminating methods and pressure assisted laminating methods.

9. - 11. (canceled)

12. (previously presented) The method of claim 16 wherein the semiconductor substrate is not thinned after forming thereover the minimum of one microelectronic device.

13. (previously presented) The method of claim 16 wherein the second substrate is not removed from the dielectric isolated metallization pattern prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern.

14. - 15. (canceled)

16. (previously presented) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication;

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication; and

removing the second substrate from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a removal method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, where the removal method employs the dielectric isolated metallization pattern as a stop layer.